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The impact of x86 instruction set architecture on superscalar processing

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Abstract

Performance improvement of x86 processors is a relevant matter. From the point of view of superscalar processing, it is necessary to complement the studies on instruction use with analogous ones on data use and, furthermore, analyze the data flow graphs, as its dependencies are responsible for limitations on ILP. In this work, using instruction traces from common applications, quantitative analyses of implicit operands, memory addressing and condition codes have been performed, three sources of significant limitations on the maximum achievable parallelism in the x86 architecture. In order to get a deeper knowledge of these limitations, the data dependence graphs are built from traces. By means of graph matrix representation, potentially exploitable parallelism is quantified and parallelism distributions from the traces are shown. The method has also been applied to measure the impact of the use of condition codes. Results are compared with previous work and some conclusions are presented relating the obtained degree of parallelism with negative characteristics of x86 instruction set architecture.

Keywords: Instruction Level Parallelism, Instruction Set Architecture, DDG-based quantification.