



Analysis of x86 Data Usage (16 bits subset)

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Análisis del uso de datos en el repertorio x86 (subconjunto de 16 bits)

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Abstract:

To study the behavior of instruction sets in the superscalar setting to analyze the data usage is necessary because the main limiting factor to parallel execution is the data dependences among instructions.

This technical report shows the data usage distribution for x86 instruction set, 16 bits subset. The work has been done with a predefined test-bench.

The detailed study of data access has been organized as follows. First of all, the explicit register usage is analyzed, next the implicit usage and finally, the status flag usage is studied.

From usage distributions for each group, quantitative results about the most important sources of potential data dependences are obtained.

Index words: Evaluation of computer architectures, instruction level parallelism, instruction set architecture.