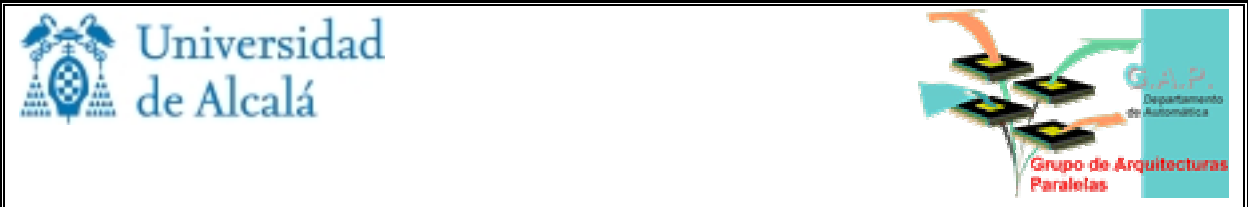

Proposal of test-bench for the x86 instruction set (16 bits subset)

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Versión en español:

Propuesta de banco de pruebas para el repertorio de instrucciones x86 (subconjunto de 16 bits)

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Abstract:

With the purpose of evaluating the instruction set architecture impact on the superscalar processing, applying a mathematical method derived from the graph theory, a set of programs is proposed as test-bench.

The application corresponds to the integer processing. The instruction set selected is the x86 one due to its peculiar characteristics with respect to instruction level parallelism.

The methodology of obtaining of execution traces is presented and the work load of each one of the selected programs.

Finally, a characterization of each program is made on the basis of his functionality and to the counts of operations and operands.

Index words: Evaluation of computer architectures, instruction level parallelism, instruction set architecture.