



## On Applying Graph Theory to ILP Analysis

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## Aplicación de la teoría de grafos al análisis del paralelismo a nivel de instrucción Nota técnica TN-UAH-AUT-GAP-2005-01-es

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## Abstract:

The differences found between the superscalar performance in x86 and non-x86 processors and the peculiar characteristics of the x86 instruction set architecture recommend to carry out a thorough analysis of the available parallelism at the machine language layer. However, computer architecture evaluation requires new tools that complement the customary simulations and, in this sense, the traditional graph theory can help to create a new frame for fine-grain parallelism analysis.

Starting off from graph theory basic foundations, new concepts are introduced from *reduced valence* to *data dependence matrix D*, both characterizing a code sequence in a mathematical manner. This matrix fulfills a number of properties and restrictions and provides information about the ability of the code to be processed concurrently. Among other details, a relation between the *critical path length* and the *parallelism degree* along with techniques to calculate it from the matrix D, are presented.

Finally, it is explained how different data dependence sources can be composed, thus providing a mechanism to analyze their final influence on the parallelism degree. These techniques are applied to an example from which some conclusions are derived.

**Index words**: Evaluation of computer architectures, instruction level parallelism, instruction set architecture, graph theory, DDG-based quantification.