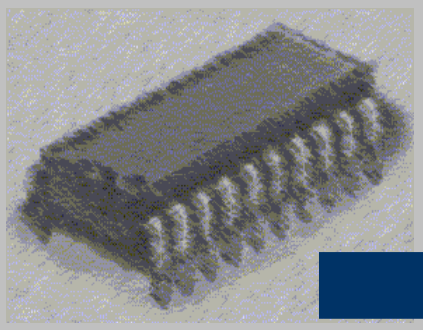
Exercises

Lesson 3: The Control Unit



Computer Structure and Organization

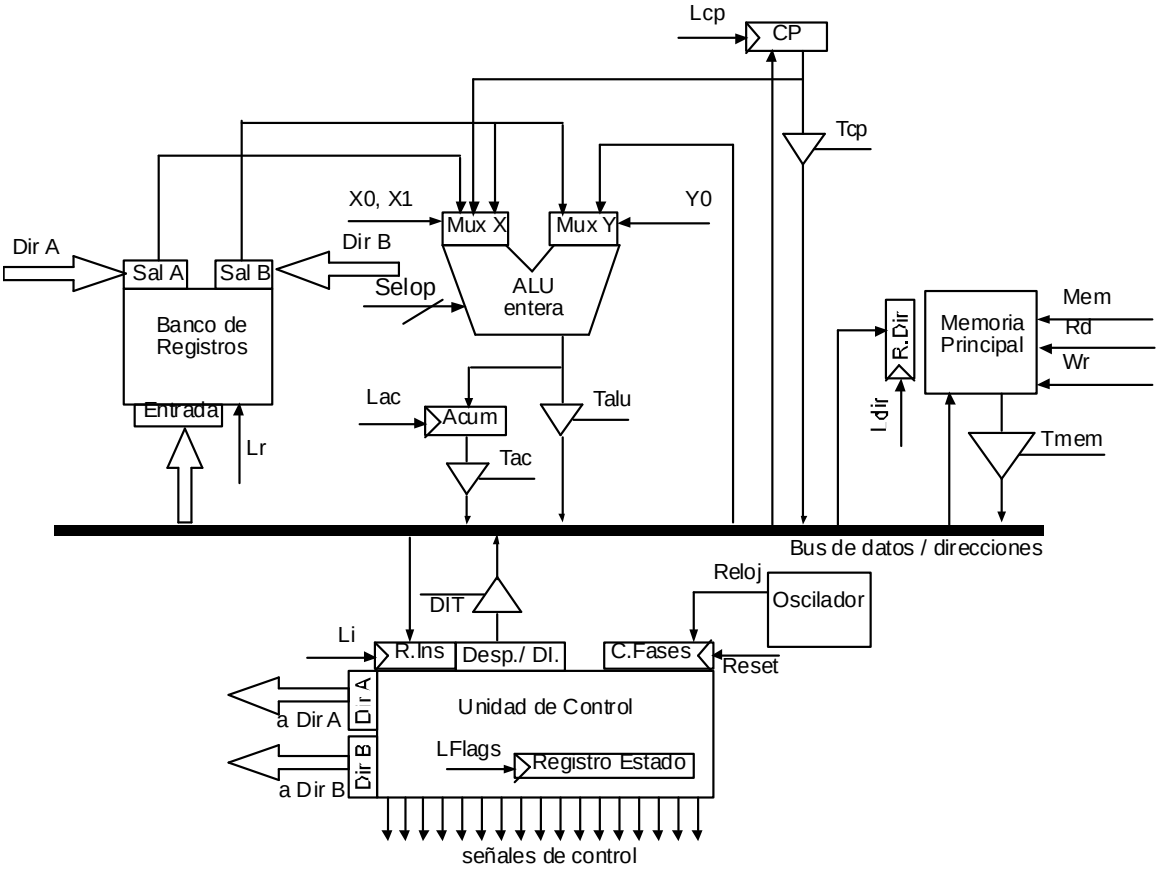
Graduate in Computer Sciences
Graduate in Computer Engineering

1. Lets be an elemental computer with the following elements:
   - A 16 operations ALU with two multiplexor attached to their inputs.
   - Accumulator register to store temporal values.
   - A 32 registers file with two outputs ports and one input port.
   - PC attached to data / addresses bus.
   - Main memory of 128 Mbytes of capacity
   - Memory reading and writing use two clock periods
   - Data / addresses bus is 32 bits length.

   Execute next instruction:

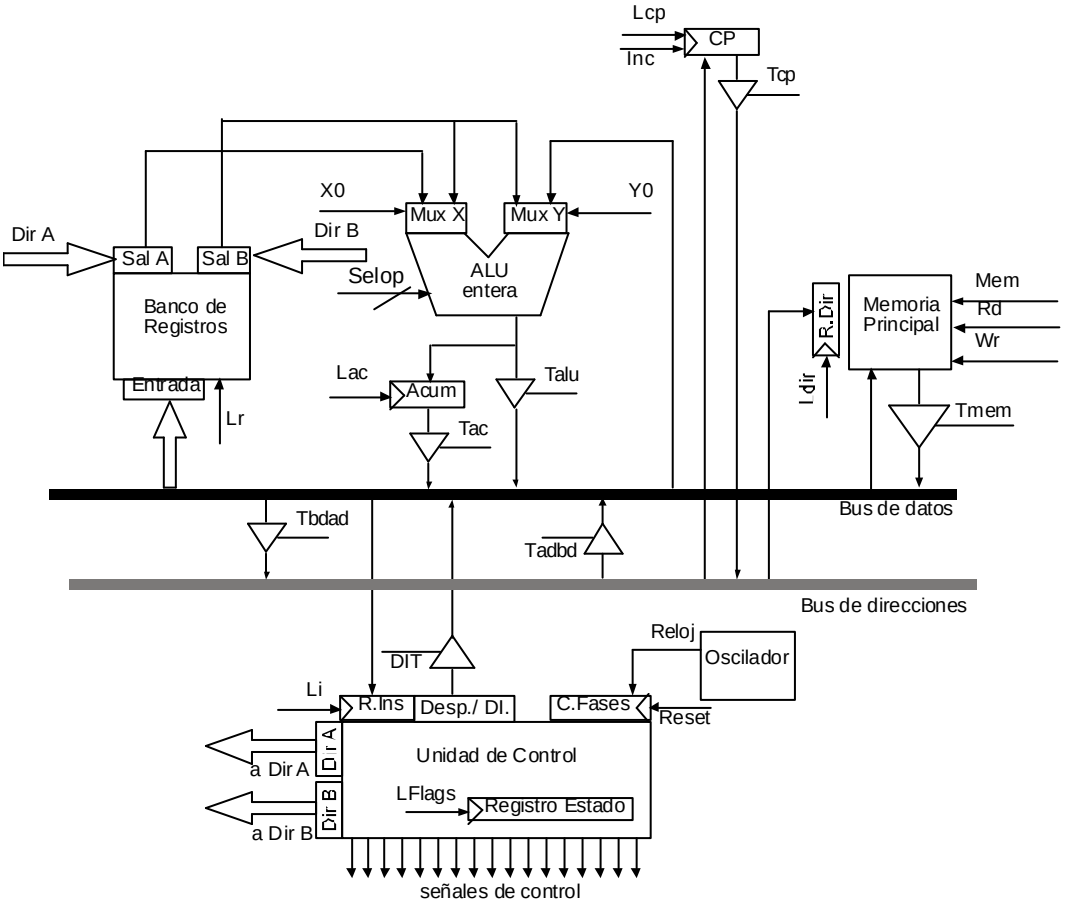
   SHL F, 5

   a. Describe elemental operation to perform in each execution phase
   b. Draw above instruction chronogram
   c. Design micro instruction format. Control Memory 64k.
   d. Design the micro program for the above execution phase.



2. Lest following elemental computer:

   - A 8 operations ALU: +, ×, arithmetic shift left and right AND, OR, XOR y logical shift right.
   - Accumulator register to store temporal values.
   - A 16 registers file with two outputs ports and one input port.
   - Autoincremented PC.
   - Main memory of 16Mbytes of capacity.
   - Data bus and addresses bus are 32 bits length.
   - All instruction formats are 4 words length.



Execute next instruction:

XOR F, [E + 1234h]

a. Describe elemental operation to perform in each execution phase

b. Draw above instruction chronogram

c. Design micro instruction format. Control Memory 64k.

d. Design the micro program for the above execution phase.

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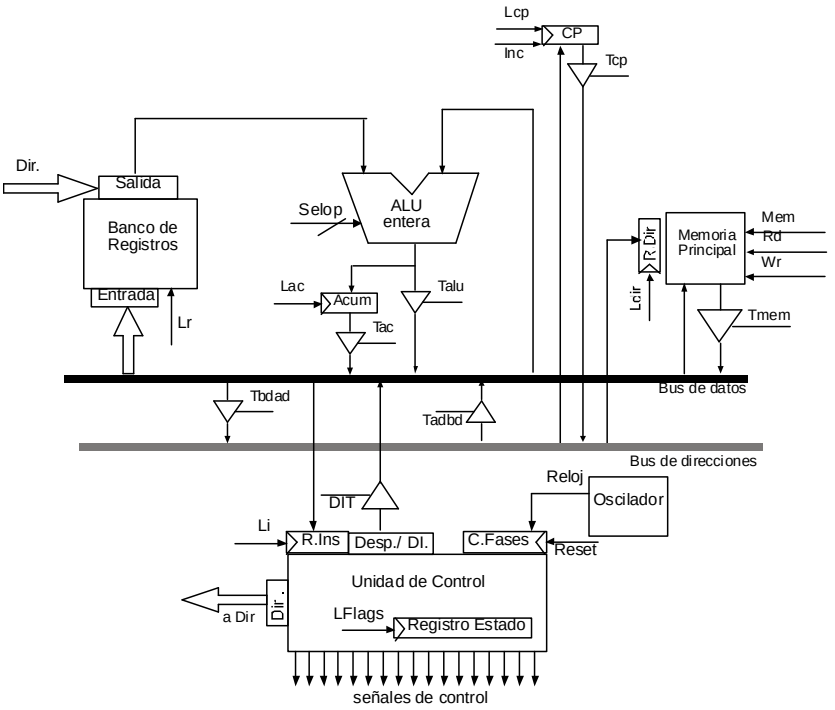
3. Lets be the following elemental computer:

- A 16 operations ALU. Input to Output transfer is one of its operations, as well ass A-B and B-A.

- Accumulator register to store temporal values.
- A 8 registers files with one input port and one output port.
- Autoincremented PC
- Main Memory of 128Mbytes of capacity.
- Data and Addresses buses are 16 bits length.
- Data bus content can be transferred to Addresses bus and vice versa.



Execute next instruction:

SUB [B++], A

a. Describe elemental operation to perform in each execution phase

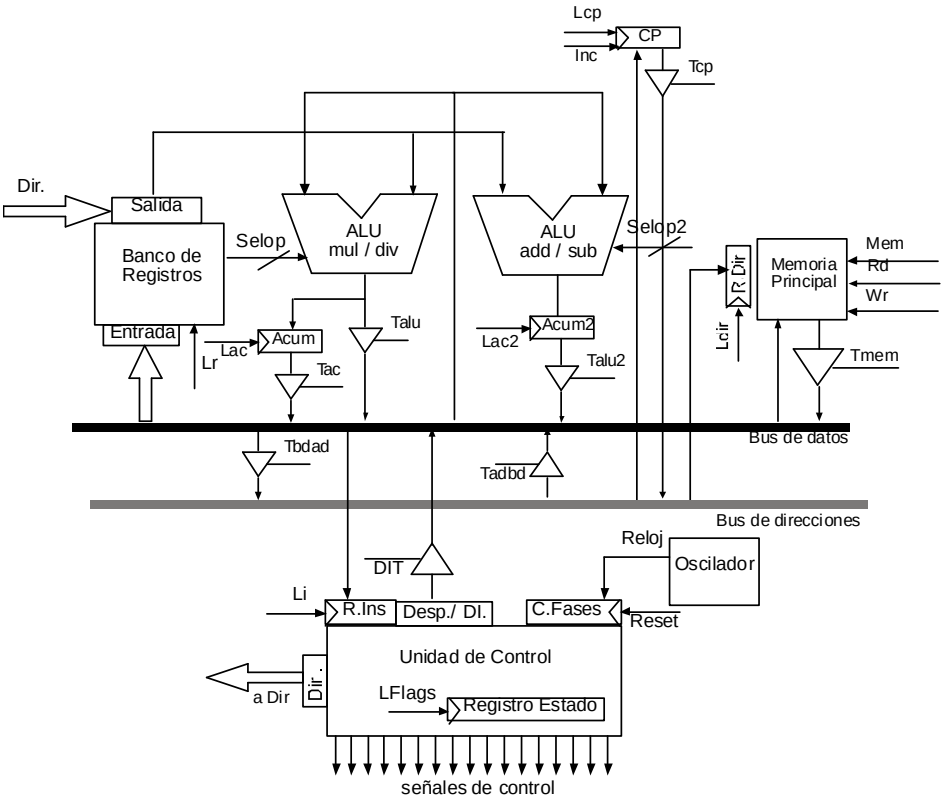
b. Draw above instruction chronogram

c. Design microinstruction format. Control Memory 32k.

d. Design the micro program for the above execution phase.

4. Lets be the following elemental computer:

   - Two ALUs: one of them is specialized in multiply and divide operations and the another one in addition and subtraction operations.
   - Both ALUs have an accumulator register to store temporal values.
   - A 32 registers file with one input port and one output port..
   - Autoincremented PC
   - Main Memory of 32Mbytes of capacity.
   - Data and Addresses buses are 32 bits length.
   - Data bus content can be transferred to Addresses bus and vice versa.
   - The whole instructions formats are 32 bits length.



Execute the following instruction:

Div C, D

a. Describe elemental operation to perform in each execution phase
b. Draw above instruction chronogram
c. Design microinstruction format. Control Memory 32k.
d. Design the micro program for the above execution phase.

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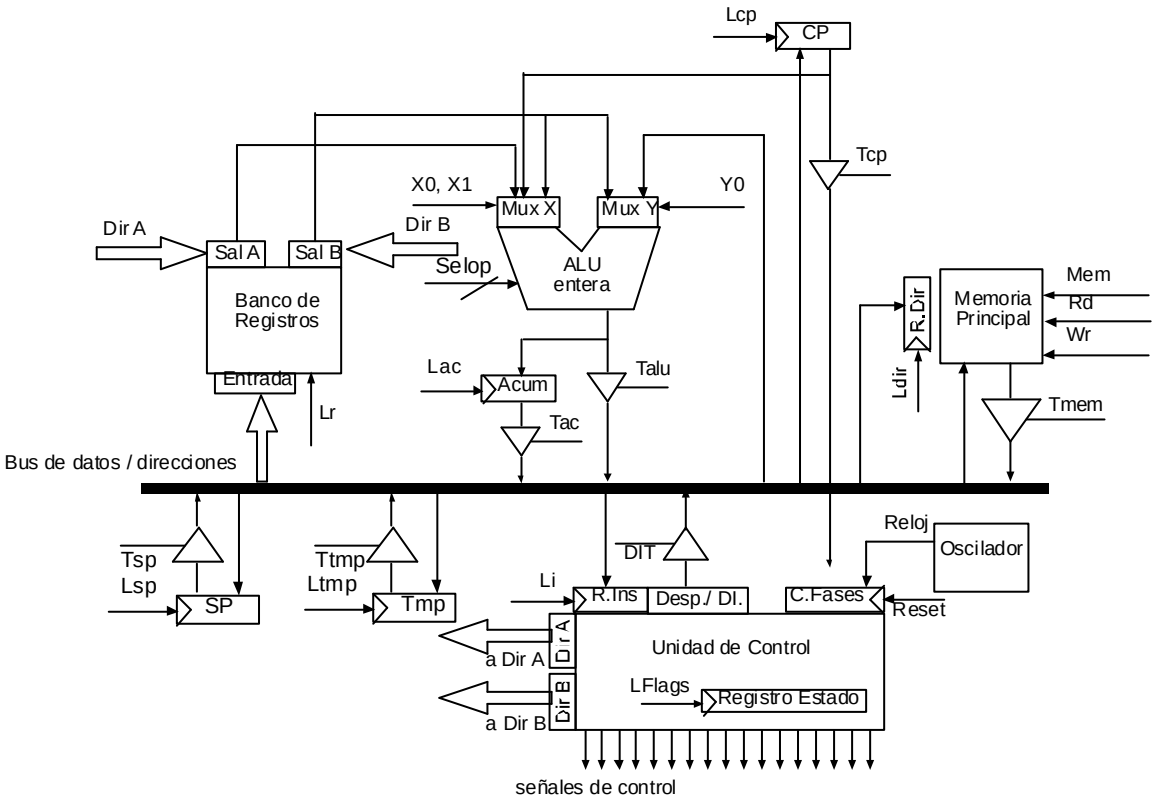
5. Lets be the next elemental computer:
    - A 32 operations ALU with the possibility of input to output transfer.
    - Temporal and Accumulator registers to store temporal values which cannot be used by assembly language.
    - 16 register files with two output ports and one input port.
    - Stack pointer attached to addresses register
    - Main memory: 16 Mbytes of capacity
    - Data bus content can be transferred to Addresses bus and vice versa.
    - Buses are 32 bits length
    - The whole instruction formats are 32 bits length.

Execute next instruction:

ADD A, B

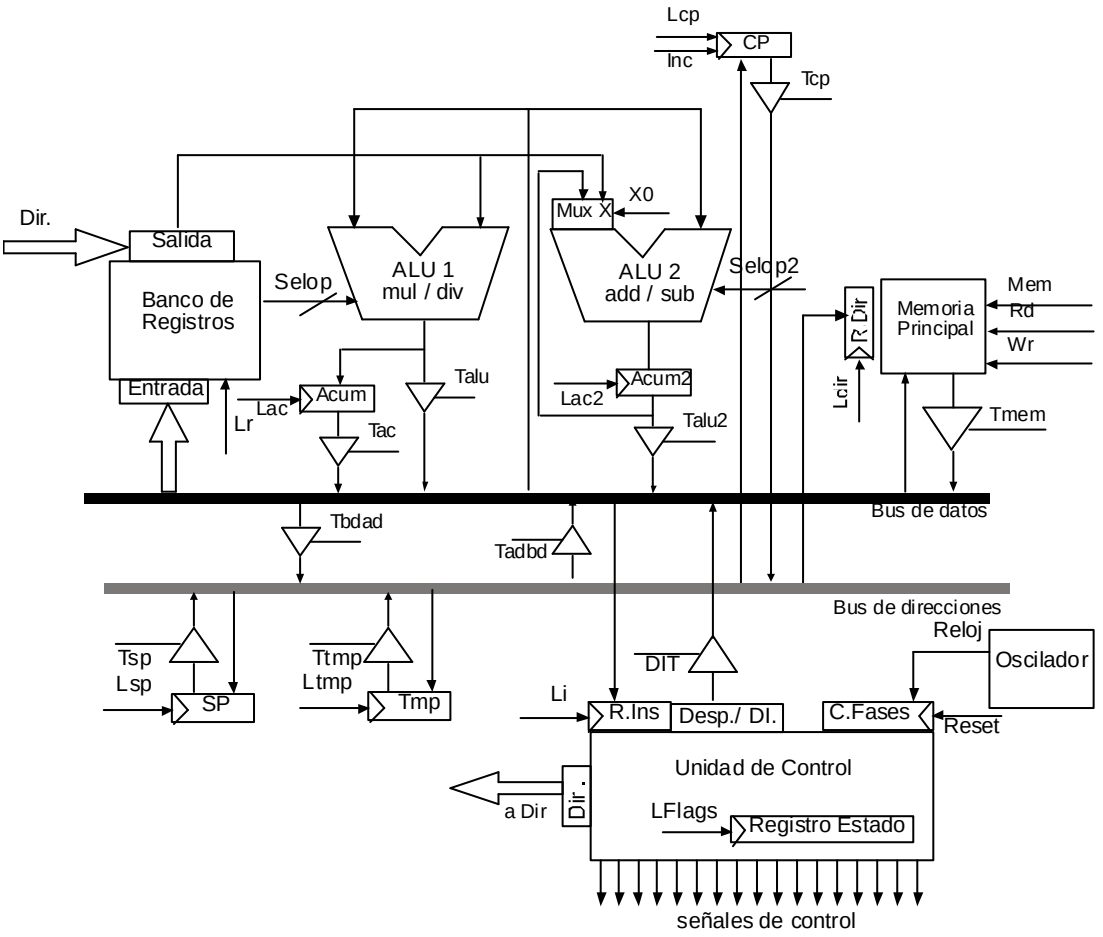
a. Describe elemental operation to perform in each execution phase
b. Draw above instruction chronogram



6. Lets be following elemental computer:

   - Two specialized ALUs: one in multiply and dicide operations, addition and subtraction the another one.
   - Temporal and Accumulator register to store temporal values with no assembly access.
   - 32 registers file with one input and output ports.
   - Autoincremented PC..
   - Stack pointer attached to addresses bus.
   - Main memory of 32Mbytes of capacity
   - Buses are 32 bits length.
   - The whole instruction formats are 32 bits length.

- Data bus content can be transferred to Addresses bus and vice versa.



Execute following isntructions:

ADD [[B + 1000h]], [C + 1234h]

a. Describe elemental operation to perform in each execution phase

b. Draw above instruction chronogram

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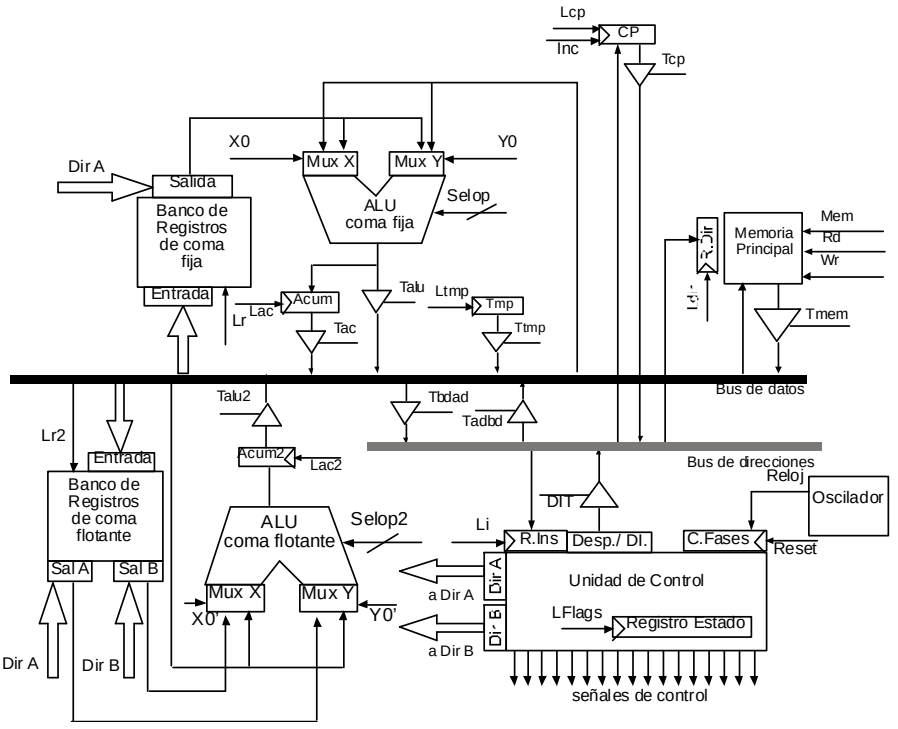
7. Lets be a elemental computer as follows.:

   - Two specialized ALUs. a fixed point ALU and a floating point one.

- Temporal and Accumulator registers to store temporal values which cannot be used by assembly language.
- Two 32 registers file with one input and output ports. One for fixed point registers and the another for floating point ones.
- Autoincremented PC
- Main Memory of 4Gbytes of capacity.
- Buses are 32 bits length.
- The whole instruction formats are 32 bits length.
- Data bus content can be transferred to Addresses bus and vice versa.



Execute following instruction:

MULF D, C, 3.27

a. Describe elemental operation to perform in each execution phase

b. Draw above instruction chronogram

8. Lets be next elemental computer:
    - A 16 operations ALU.
    - 3 registers file: B, C and D.
    - Main Memory of 640Kbytes.
    - Data and Addresses buses are 32 bits length

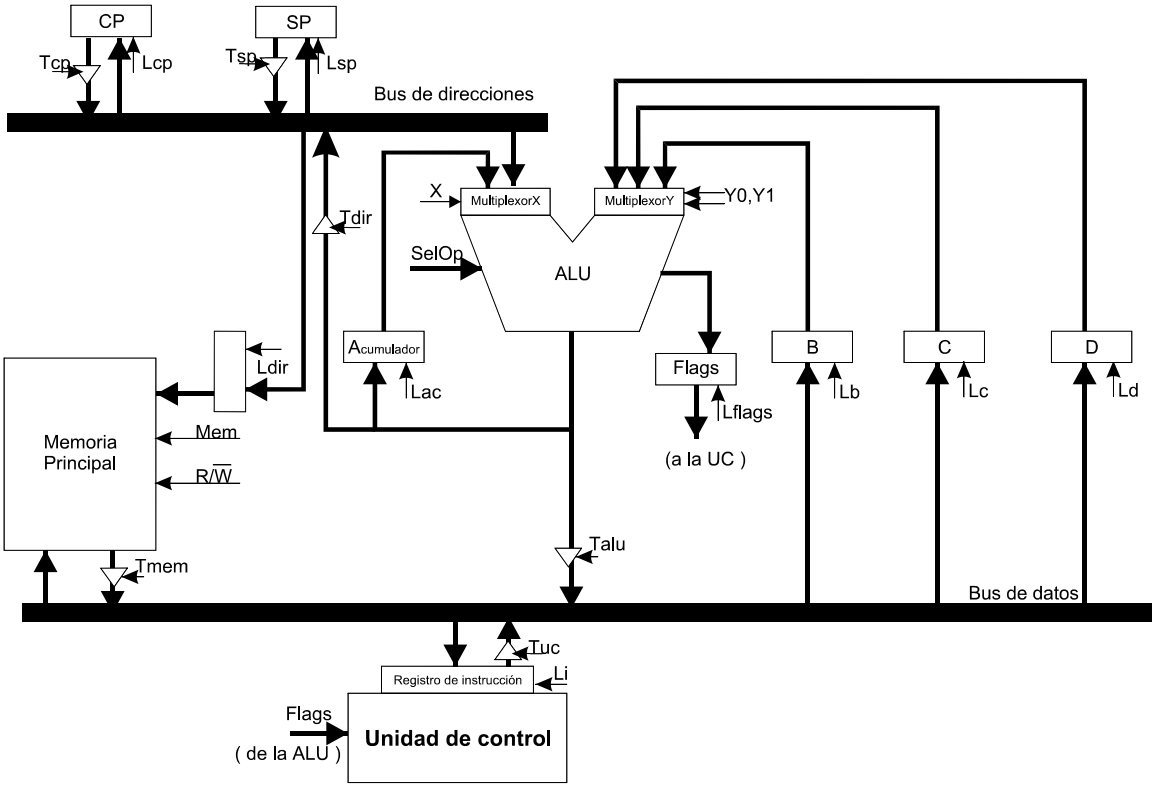
Execute following instruction:

SUB B, [C + 1000h]

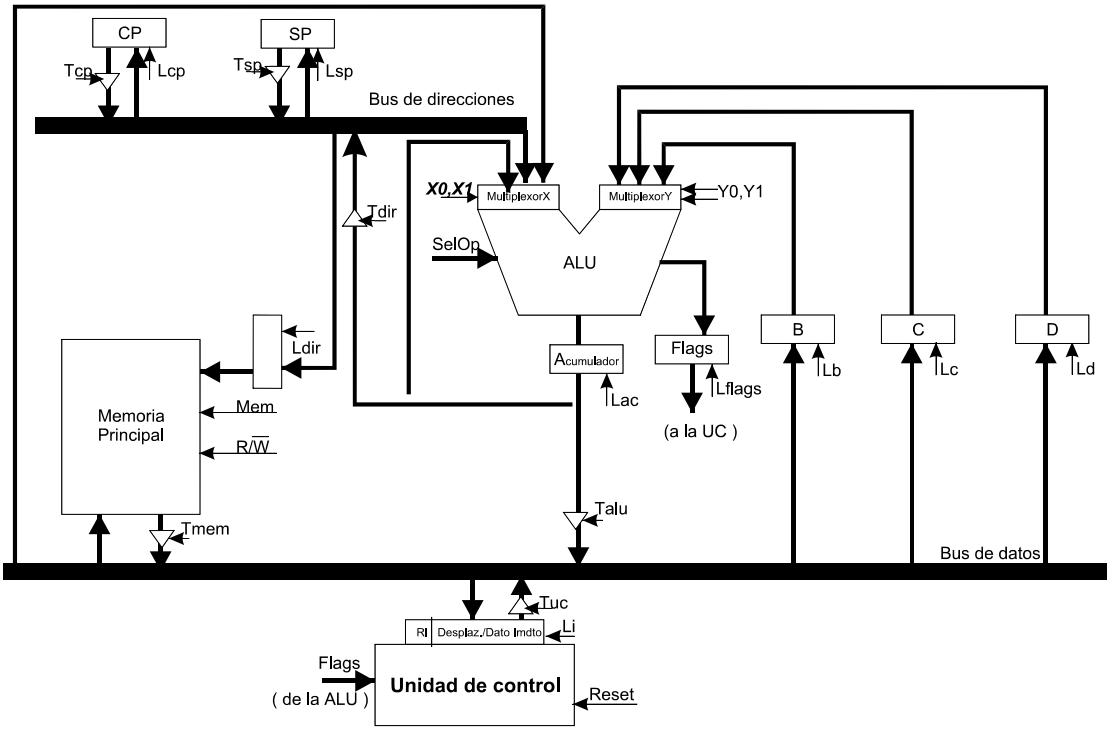
a. Modify bellow computer if needed

b. Describe elemental operation to perform in each execution phase

c. Draw above instruction chronogram



9. Lets be following elemental computer:
    - A 16 operations ALU.
    - Datapath contains PC, SP and Accumulator register, as well as a 3 registers file.
    - Main memory 32 Kbytes of capacity.
    - Data bus: 8 bits.
    - Addreses bus: 16 bits.
    - Instructions have different sizes



Execute next instruction:

POP B

a. Describe elemental operation to perform in each execution phase
b. Draw above instruction chronogram