

PRACTICE 3

Assembly and evaluation of combinational digital systems.

1. Objectives

The aim of the following exercise is to familiarize students with combinational systems management:

- • Handle the truth tables defining the combinational systems.
- • Mount and connect C.I. digital as orderly as possible.
- • Debugging the circuit using the instruments available in the laboratory.
- • Know the most used systems of data visualization.

2. Materials required

Besides the common material 2 shown in practice will need the following components:

- 74157 Quadruple two-input multiplexer.
- 7485 Comparator of two 4-bit numbers.
- 7447 Decoder BCD to seven segments.
- 7483 Adder (required for improvement).
- Display of common anode. There are many models with pretty price change (5150, 7650, 7651, 7750, etc.). Any of them is valid whenever it is common anode.
- 8 LED diodes.
- DIP: 2 units of 4 microswitches each or 1 unit of 8 microswitches.
- Resistors: 8 units of 1 K Ω y and 8 units of 330 Ω .

View the datasheet:

[.http://atc2.aut.uah.es/~rosa/Fundamentos/laboratorioFtos.htm#Material](http://atc2.aut.uah.es/~rosa/Fundamentos/laboratorioFtos.htm#Material)

Or search:

www.datasheetcatalog.com

3. Previous concepts

The student must have clear the concepts studied in theory classes about combinational systems: truth tables, canonical functions, simplifying functions, etc., and the functioning of all integrated combinational circuits that are used in this practice.

4. Questions

Before carrying out the practice, each group member must answer the following questions **individually** and deliver them to the teacher. This requires reading the full statement of the practice and see the datasheet of the integrated circuits

<http://atc2.aut.uah.es/~rosa/Fundamentos/laboratorioFtos.htm#Material>

O buscar en www.datasheetcatalog.com

- Questions relating to **multiplexer**:

a) Which is its function?

b) What is the purpose of the terminal "Select"?

c) What value should be put in the input "Strobe"?

- Questions relating to **comparator**:

a) What is the purpose of the cascading inputs? If you compare numbers of 4 bits, and you want to activate the output $A = B$ only when they are equal. In what way you will have to connect the cascading inputs?

b) What value will have the comparator outputs when data A is greater than data B?

- Issues related to the **logical connection between the comparator and the multiplexer:**

a) Complete the following truth table corresponding to the logical connection between the comparator and the multiplexer. It must indicate, in the different cases (where data are equal or one data is greater than the other), which outputs are provided by the comparator, which is the data to be displayed, and what is the select to be entered in the multiplexer to display that data.

Data	Comparator outputs			Data to be showed	Select
	A>B	A=B	A<B		
Data A > Data B					
Data A = Data B					
Data B > Data A					

Table 1. Table corresponding to the logical connection.

5. Development of practice

The ultimate goal of this practice is the realization of a digital system having as input two binary numbers in 4-bit BCD (**A** and **B**) and visualize on a display the greater of the two. To carry out the practice should follow the steps outlined below. Steps are **cumulative**, ie, to perform each do not disassemble the previous, but add new components to the previous system.

NOTE: Before mounting each step is advised to implement the logic circuit on paper, with the help of the accompanying features. These pictures will help you understand the complete functioning of the system.

5.1. Mounting the multiplexer

Mount the multiplexer using microswitches to enter the two input data. Take the control signal directly to Vcc or ground. Use as many LEDs as necessary to display all outputs of the multiplexer. Check operation of this step, selecting a different value for A and B, and multiplexing to see each of the two binary codes to the output. (Follow the notes of laboratory **item 2** Connecting the microswitch and LED)

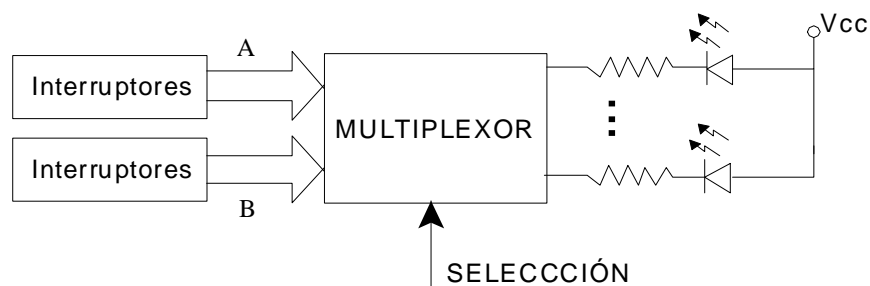


Figure 1. Mounting block diagram of the multiplexer.

5.2. Mounting the Comparator

Without removing the previous circuit, and using the same data (microswitches) for introducing the input comparator circuit, mount the circuit shown in figure 2. Consider that for the data entered in the multiplexer and in the comparator are the same, the cables that go to the multiplexer data A (or B), must also go to the same data A (or B) in the comparator. They must go in the same order. Note that in the data sheet of both components different nomenclature are used: in the comparator the least significant bit is A0 while in the multiplexer is A1, and so on.

The control inputs of the comparator are "cascading inputs" and its value must be such that when the values of A and B are equal, the circuit outputs indicate that the input data are the same (see the data sheet). Use LEDs to display outputs.

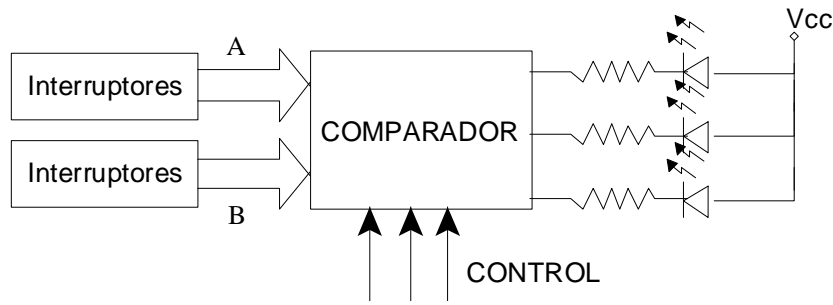


Figure 2. Mounting block diagram of the comparator.

5.3. Logical connection between multiplexer and comparator

Design the logic required between the comparator and the multiplexer so that the output of the multiplexer is the higher of the two numbers.

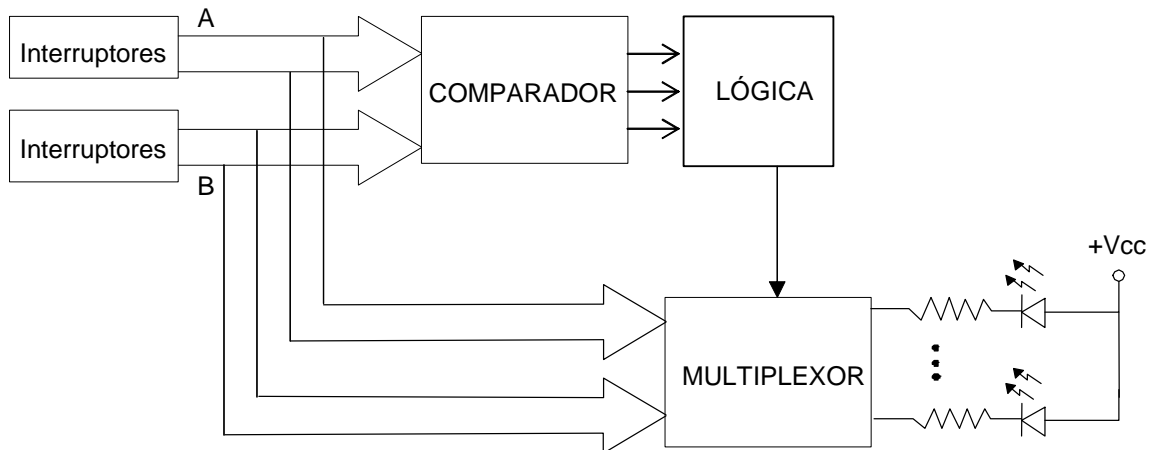


Figure 3. block diagram circuit that selects the greater of two numbers.

Design the logic (the simpler the better) to generate the multiplexer control signal that will show the number greater of the two. The logic inputs of this block are the comparator outputs.

5.4. Mounting the display circuit

Without removing the previous circuit, design and assemble a display system that represents the output of the multiplexer (BCD number one digit) in a 7-segment display. You should take into account the type of display, the mode of connection of the resistance of each segment, the BCD-7 segment decoder used, etc. Follow laboratory item 2 notes on Visualization “using a common anode display” in the design of this part of the circuit. Draw into the space of Figure 4, the design of relative to this stage from the outputs of the multiplexer.

Figure 4. Block diagram of the visual stage.

6. Improvement (Optional)

Redesign the system (changing the necessary components and their connections) to output to display the sum of the two inputs, $A + B$, where the result is a number between 0 and 9.