



Exam of Fundamentals of Computer Technology. Grados en I. Computadores I. Informática. English group

SURNAMES: Name:

	Test 4 pts.	Right answer ⇒ 0,4	Wrong ⇒ - 0,1	No answer ⇒ 0
1) 	Point the WRONG statement 1Gbyte is 2 ¹⁰ Kbytes 1Mbyte is 2 ²⁰ bytes 1Kbyte is 2 ¹⁰ bytes 1 byte is 2 ³ bits			
2) 	Which is the I XOR AND OR XNOR	ogical gate that produces "1	" as output JUST wh	en the two inputs are equal?
3) 	Fetch inst Update Po Fetch inst	execution cycles in a Von Naruction, decode, fetch opera C, decode, fetch instruction rruction, decode, fetch opera ne previous options is corre	and, execution, store , fetch operand, exec and, update PC, exec	results, update PC ution, store results
4) 	It is the sa It facilitate	uage: of mnemonics or symbolic rame for all computers as the portability of program ne previous options is corre	s	
5) 	significant bit To the clo To the ou To the ou	connected to?	ores the second leas tores the second leas	
6) [] [] []	228 -27 -228	ecimal value of the C1 numbers		
7) 	382 -127 126	11 y B=111111111 are repre		m A + B has the decimal value::
8) [] [] []	S = A!B!C S = ABCL S = ABCL	nonical forms of the function CD + ABCD D + A!B!C!D! + A!B!CD + A D + A!B!CD + A!BCD + AB ne previous options is corre	ABC!D! ICD	:
9) 	What value do $Q^{t+1}=0$ $Q^{t+1}=1$ $Q^{t+1}=Q^{t}$ $Q^{t+1}=Q^{t}$	oes the output of a bistable	JK take when J=1, K	=0, is connected to the input?
10) 	The syste The syste The syste	n address a 256M x 32 mer m has a 29-line data bus ar m has a 32-line data bus ar m has a 27-line data bus ar	nd a 32-line address b nd a 29-line address b nd a 32-line address b	ous.



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EXERCISE 1 (2 points)

A simple geopositioning system consists of 4 satellites. Design a circuit for the terrestrial receiver that warns by turning on a LED when it receives the signal from at least 3 satellites and therefore can correctly calculate the position (assume that each of the signals received correctly from the satellites produces a "1" at the input of the circuit to be designed).

Exa Gra

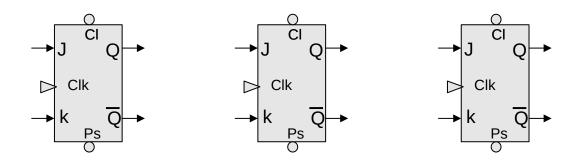
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EXERCISE 2 (2 points)

Make the connections in the following diagram to build a counter that follows the sequence 0, 5, 2, 6. Add the necessary logic gates

Vcc

Gnd



Clk

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EXERCISE 3 (2 points)

In a CPU with 64 bits in the data bus and 30 bits in the address bus it is required to install a memory system with the following characteristics:

- 512M x 64 of RAM memory in the higher memory positions
- 256M x 64 of ROM memory in the lower memory positions

For that purpose an unlimited amount of the following chips are available:

- 256M x 64 memory chips
- 256M x 32 ROM memory chips
- a) Draw the memory map indicating the first and the last address of each chip.
- b) Indicate the connections to the CS input of each chip.